TFT LCD Preliminary Specification

MODEL NO.: N133I6 - P0A

Customer:

Approved by:

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
1.0	Dec, 04,'09	All	All	Preliminary specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N133I6 - P0A is a 13.3" TFT Liquid Crystal Display open cell with a 40 pins LVDS interface. This open cell supports 1280 x 800 WXGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The converter open cell for Backlight is built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA (1280 x 800 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATI0NS

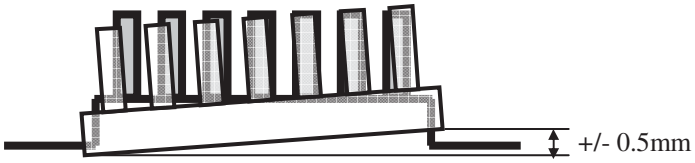
Item	Specification	Unit	Note
Active Area	286.08 (H) x 178.8 (V)	mm	(1)
Top Polarizer Area	289.48 (H) x 182.2 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.2235 (H) x 0.2235 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Anti Glare	-	-

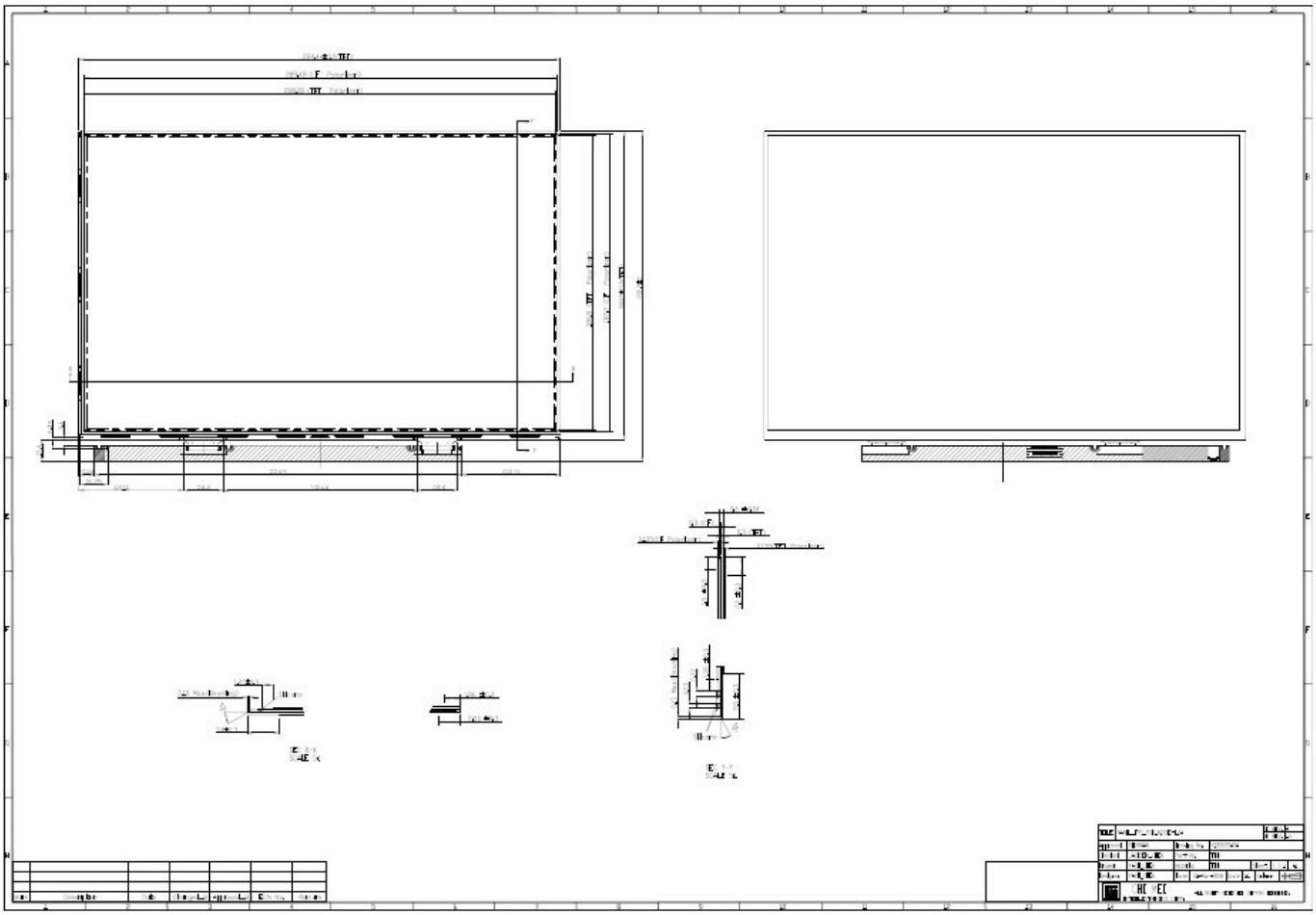
1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	**Horizontal (H)**	**294.24**	**294.44**	**294.64**	**mm**	(1) (2)
	Vertical (V) With PCB	**200.9**	**201.9**	**202.9**	**mm**	
	Vertical (V) W/o PCB	**188.3**	**188.5**	**188.7**	**mm**	
	Thickness (T) With PCB	**3.45**	**3.6**	**3.75**	**mm**	
	Thickness (T) W/o PCB	**0.77**	**0.87**	**0.97**	**mm**	
Weight		-	-	**175**	**mm**	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position





2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)

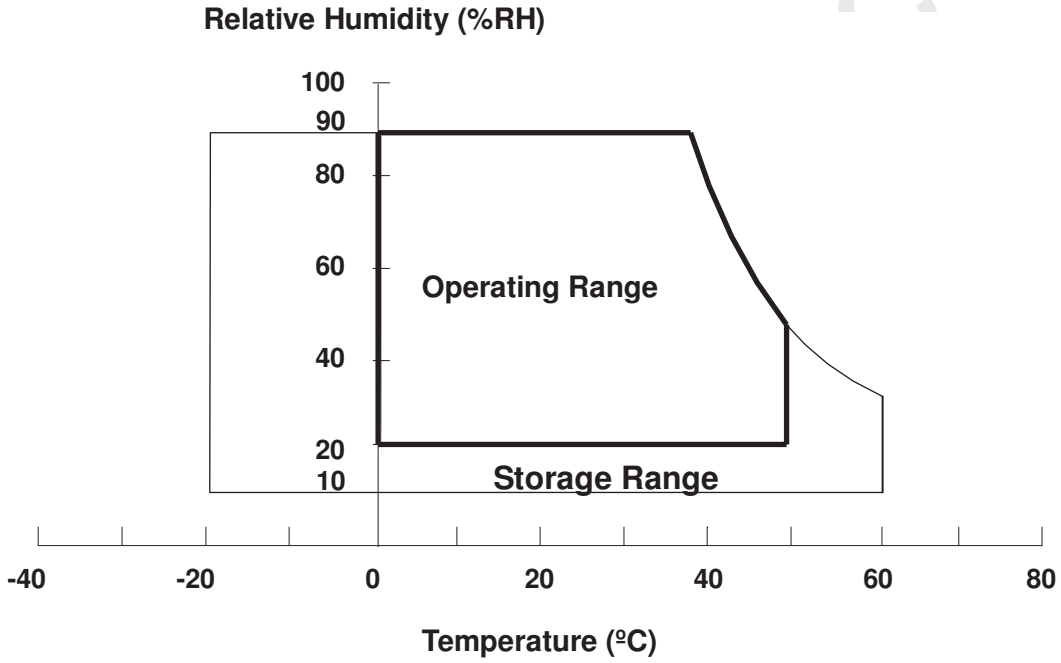
Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be 0 ºC Min. and 50 ºC Max.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

High temperature or humidity may reduce the performance of panel. Please store LCD panel within the specified storage conditions.

Storage Condition: With packing.

Storage temperature range: 25±5 ºC.

Storage humidity range: 50±10%RH.

Shelf life: 30days

2.2 ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	V_{CC}+0.3	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD OPEN CELL

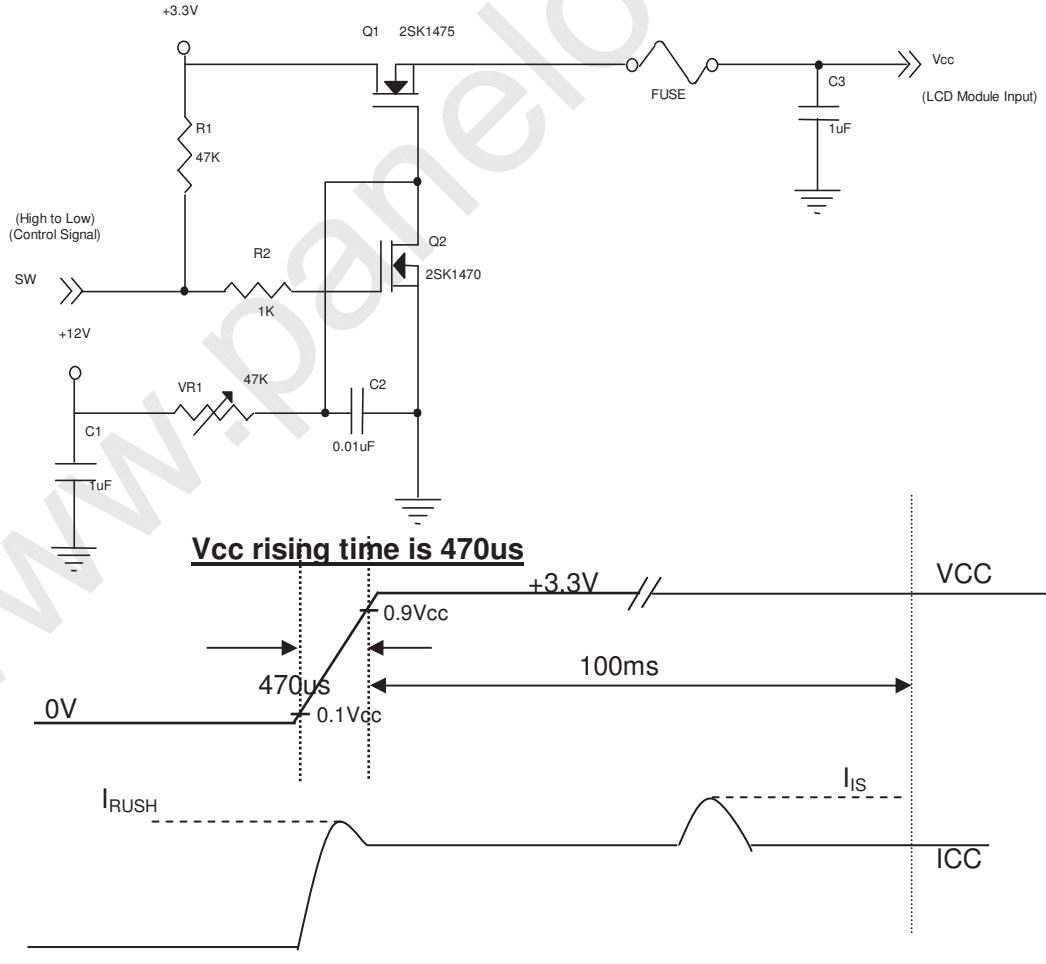
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	3.0	3.3	3.6	V	-
Permissive Ripple Voltage		V_{RP}	-	50	-	mV	-
Rush Current		I_{RUSH}	-	-	1.5	A	(2)
Initial Stage Current		I_{IS}	-	-	1.0	A	(2)
Power Supply Current	White	Icc	-	200	230	mA	(3)a
	Black		-	270	300	mA	(3)b
LVDS Differential Input High Threshold		$V_{TH(LVDS)}$	-	-	+100	mV	(5), V_{CM}=1.2V
LVDS Differential Input Low Threshold		$V_{TL(LVDS)}$	-100	-	-	mV	(5) V_{CM}=1.2V
LVDS Common Mode Voltage		V_{CM}	1.125	-	1.375	V	(5)
LVDS Differential Input Voltage		$\|V_{ID}\|$	100	-	600	mV	(5)
Terminating Resistor		R_T	-	100	-	Ohm	
Power per EBL WG		P_{EBL}	-	1.4	-	W	(4)

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

Note (2) I_{RUSH}: the maximum current when VCC is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

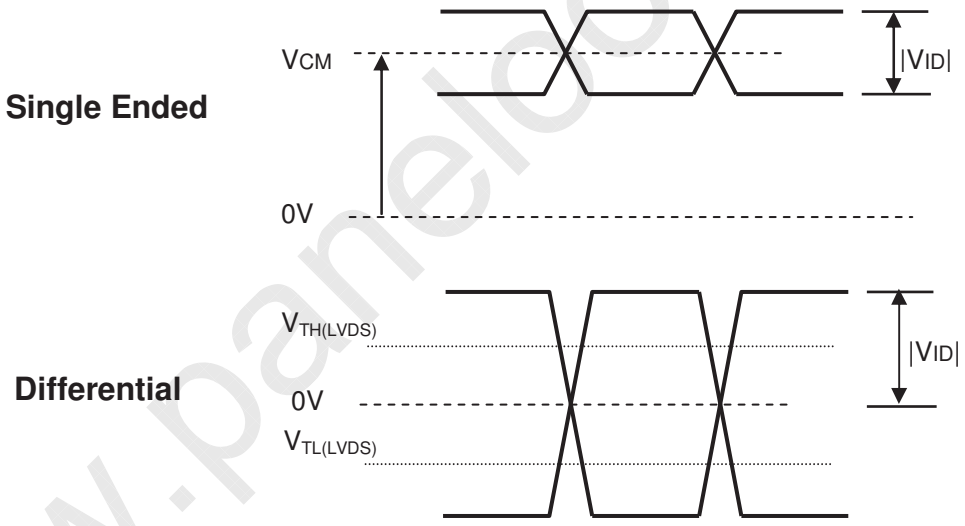
a. White Pattern

Active Area

b. Black Pattern

Active Area

Note (4) The parameters of LVDS signals are defined as the following figures.



Note (5) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

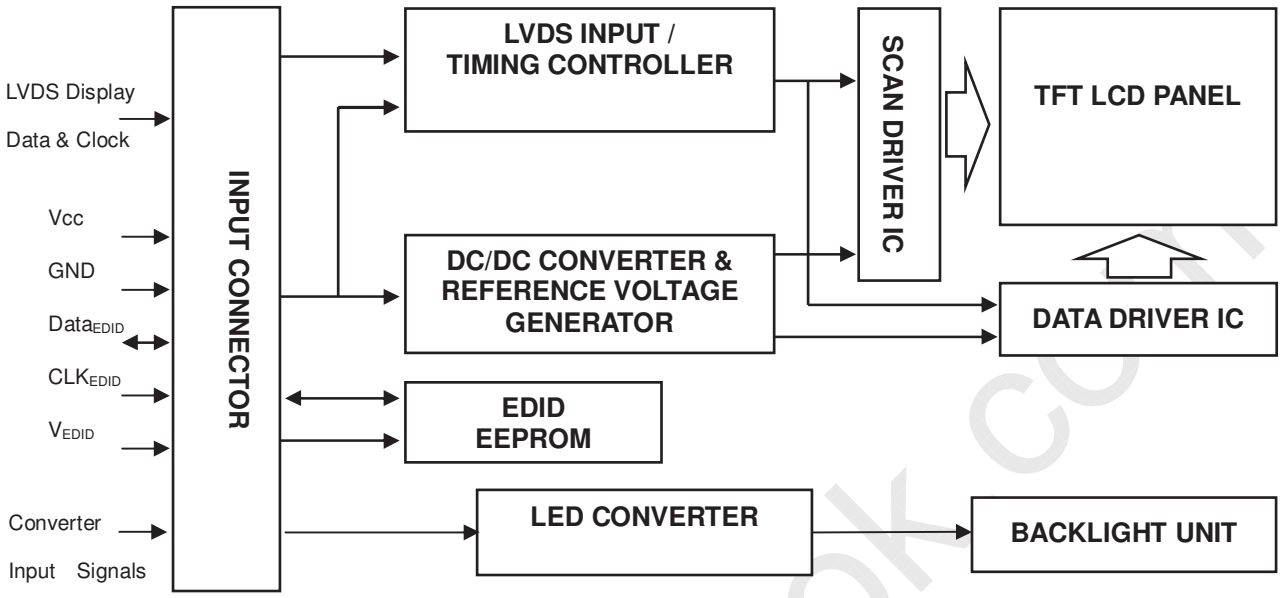
(a) VCCS = 3.3 V, Ta = 25 ± 2 ºC, f_v = 60 Hz,

(b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.

(c) Luminance: 60 nits.

4. BLOCK DIAGRAM

4.1 TFT LCD OPEN CELL



5. INPUT TERMINAL PIN ASSIGNMENT

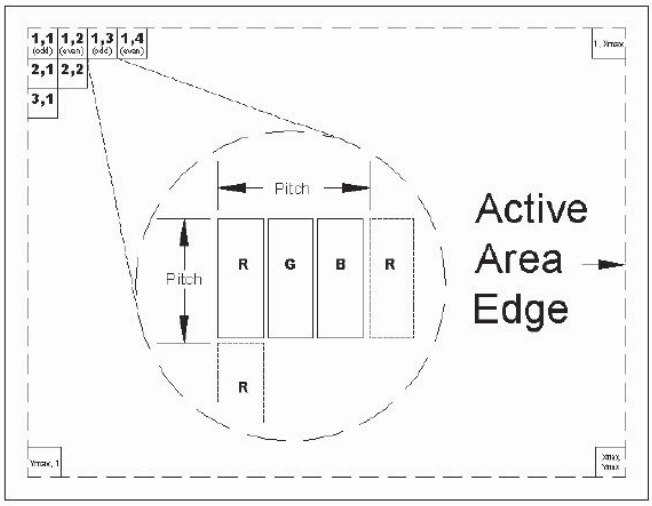
5.1 TFT LCD OPEN CELL

Pin	Symbol	Description	Polarity	Remark
1	VSS	Ground		
2	NC	no connect		
3	VDD	Logic power 3.3V		
4	VDD	Logic power 3.3V		
5	VDD	Logic power 3.3V		
6	VEDID	EDID 3.3V power		DDC 3.3V Power
7	NC	no connect		
8	CLK	EDID clock		DDC Clock
9	DATA	EDID data		DDC Data
10	VSS	Ground		
11	VSS	Ground		
12	NC	no connect		
13	RIN0-	- LVDS differential data input (R0-R5, G0)	Negative	R0~R5,G0
14	RIN0+	+ LVDS differential data input (R0-R5, G0)	Positive	
15	VSS0	Ground-LVDS0		
16	RIN1-	- LVDS differential data input (G1-G5, B0-B1)	Negative	G1~G5, B0, B1
17	RIN1+	+ LVDS differential data input (G1-G5, B0-B1)	Positive	
18	VSS1	Ground-LVDS1		
19	RIN2-	- LVDS differential data input (B2-B5,HS,VS, DE)	Negative	B2~B5, DE, Hsync, Vsync
20	RIN2+	+ LVDS differential data input (B2-B5,HS,VS, DE)	Positive	
21	VSS2	Ground-LVDS2		
22	CLK-	- LVDS differential clock input		LVDS Level Clock
23	CLK+	+ LVDS differential clock input		
24	VSS3	Ground-LVDS3		
25	INV_PWM / R_PWM	PWM brightness control		
26	LED_Enable	Enable LED		
27	VSS	LED Ground		
28	VSS	LED Ground		
29	VSS	LED Ground		
30	VSS	LED Ground		
31	NC	no connect		
32	VBL+	7V - 20V LED power		
33	VBL+	7V - 20V LED power		
34	VBL+	7V - 20V LED power		
35	VBL+	7V - 20V LED power		
36	VBL+	7V - 20V LED power		
37	NC	no connect		
38	NC	no connect		
39	NC	no connect		
40	VSS	Ground		

Note (1) Connector Part No.: 20347- 140E-02(I-PEX) or equivalent

Note (2) User's connector Part No: 20345-040T-02 (I-PEX) or equivalent

Note (3) The first pixel is odd as shown in the following figure.

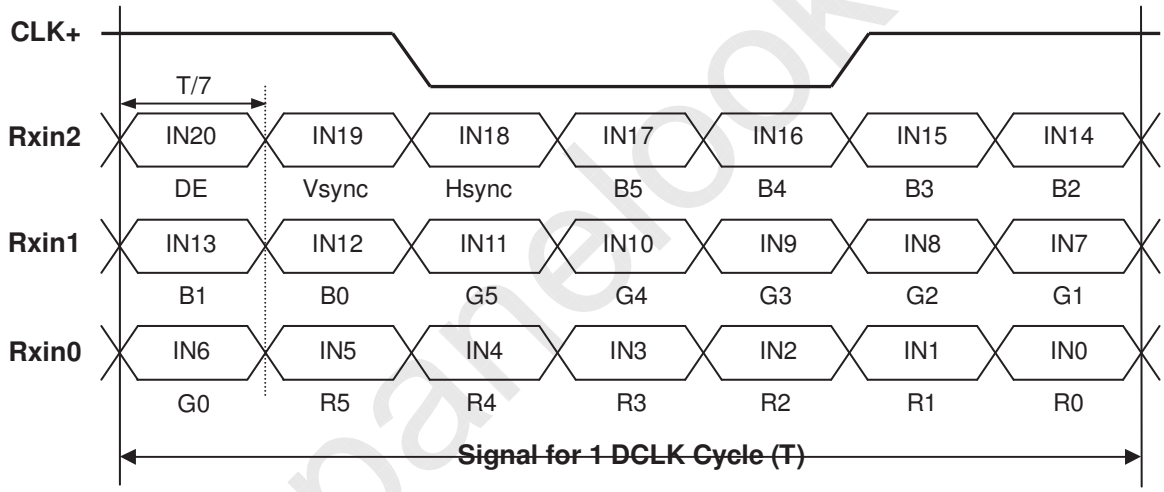


5.2 LED CONVERTER OUTPUT PIN ASSIGNMENT

Pin	Symbol	Description
1	CH1	LED converter feedback channel 1
2	NC	No connection
3	CH2	LED converter feedback channel 2
4	NC	No connection
5	NC	No connection
6	NC	No connection
7	V_L	LED converter output voltage
8	V_L	LED converter output voltage

Note (1) Connector Part No.: ???? or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name (“CMO”)	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N133I6-L0A)	13	00010011
11	0B	ID product code (hex LSB first; N133I6-L0A)	13	00010011
12	0C	ID S/N (fixed “0”)	00	00000000
13	0D	ID S/N (fixed “0”)	00	00000000
14	0E	ID S/N (fixed “0”)	00	00000000
15	0F	ID S/N (fixed “0”)	00	00000000
16	10	Week of manufacture (fixed week code)	23	00100011
17	11	Year of manufacture (fixed year code)	12	00010010
18	12	EDID structure version # (“1”)	01	00000001
19	13	EDID revision # (“3”)	03	00000011
20	14	Video I/P definition (“digital”)	80	10000000
21	15	Active area horizontal 28.608cm	1D	00011101
22	16	Active area vertical 17.88cm	13	00010011
23	17	Display Gamma (Gamma = ”2.2”)	78	01111000
24	18	Feature support (“Active off, RGB Color”)	0A	00001010
25	19	Red/Green (Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0)	5C	01011100
26	1A	Blue/White (Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0)	80	10000000
27	1B	Red-x (Rx = “0.622”)	98	10011000
28	1C	Red-y (Ry = “0.346”)	58	01011000
29	1D	Green-x (Gx = ”0.333”)	51	01010001
30	1E	Green-y (Gy = ”0.528”)	8E	10001110
31	1F	Blue-x (Bx = ”0.164”)	27	00100111
32	20	Blue-y (By = ”0.162”)	25	00100101
33	21	White-x (Wx = ”0.313”)	50	01010000
34	22	White-y (Wy = ”0.329”)	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer’s reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001

40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“71MHz”, According to VESA CVT Rev1.1)	BC	10111100
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active (“1280”)	00	00000000
57	39	# 1 H blank (“160”)	A0	10100000
58	3A	# 1 H active : H blank (“1280 : 160”)	50	01010000
59	3B	# 1 V active (”800”)	20	00100000
60	3C	# 1 V blank (”23”)	17	00010111
61	3D	# 1 V active : V blank (”800 :23”)	30	00110000
62	3E	# 1 H sync offset (”48”)	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width (”3 : 6”)	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”48: 32 : 3 : 6”)	00	00000000
66	42	# 1 H image size (”286 mm”)	1E	00011110
67	43	# 1 V image size (”179 mm”)	B3	10110011
68	44	# 1 H image size : V image size (”286 : 179”)	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	19	00011001
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name “N133I6-L0A”, ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name (“N”)	4E	01001110
78	4E	# 2 2nd character of name (“1”)	31	00110001
79	4F	# 2 3rd character of name (“3”)	33	00110011
80	50	# 2 4th character of name (“3”)	33	00110011
81	51	# 2 5th character of name (“I”)	49	01001001
82	52	# 2 6th character of name (“6”)	36	00110110
83	53	# 2 7th character of name (“-”)	2D	00101101
84	54	# 2 8th character of name (“L”)	4C	01001100

85	55	# 2 9th character of name (“0”)	30	00110000
86	56	# 2 9th character of name (“A”)	41	01000001
87	57	# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with “Blank” character	20	00100000
89	59	# 2 Padding with “Blank” character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor “CMO”, ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 1st character of string (“C”)	43	01000011
96	60	# 3 2nd character of string (“M”)	4D	01001101
97	61	# 3 3rd character of string (“O”)	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with “Blank” character	20	00100000
100	64	# 3 Padding with “Blank” character	20	00100000
101	65	# 3 Padding with “Blank” character	20	00100000
102	66	# 3 Padding with “Blank” character	20	00100000
103	67	# 3 Padding with “Blank” character	20	00100000
104	68	# 3 Padding with “Blank” character	20	00100000
105	69	# 3 Padding with “Blank” character	20	00100000
106	6A	# 3 Padding with “Blank” character	20	00100000
107	6B	# 3 Padding with “Blank” character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name“N133I6-L0A”, ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name (“N”)	4E	01001110
114	72	# 4 2nd character of name (“1”)	31	00110001
115	73	# 4 3rd character of name (“3”)	33	00110011
116	74	# 4 4th character of name (“3”)	33	00110011
117	75	# 4 5th character of name (“I”)	49	01001001
118	76	# 4 6th character of name (“6”)	36	00110110
119	77	# 4 7th character of name (“-”)	2D	00101101
120	78	# 4 8th character of name (“L”)	4C	01001100
121	79	# 4 9th character of name (“0”)	30	00110000
122	7A	# 4 9th character of name (“A”)	41	01000001
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with “Blank” character	20	00100000
125	7D	# 4 Padding with “Blank” character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	2D	00101101

6 CONVERTER SPECIFICATION

6.1 ABSOLUTE MAXIMUM RATINGS

Symbol	Ratings
Vin	40.0V
Gnd	+/-0.3V
PWM, EN	-0.3V~6.0V

6.2 RECOMMENDED OPERATING RATINGS

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		V_{in}	7.0	12.0	21.0	V	
EN Control Level	Backlight on		2.0	---	5.5	V	
	Backlight off		0	---	0.8	V	
PWM Control Level	PWM High Level		2.0	---	5.5	V	
	PWM Low Level		0	---	0.8	V	
PWM Control Duty Ratio			20		100	%	
PWM Control Frequency		f_{PWM}	180	200	220	Hz	
Converter Input Current	Vin=7 V	I_{BL}		600	650	mA	(1)
	Vin=21V			200	220	mA	(2)

Note (1) The specified LED power supply current is under the conditions at Vin = 7 V, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

Note (2) The specified LED power supply current is under the conditions at Vin = 21V, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

7. INTERFACE TIMING

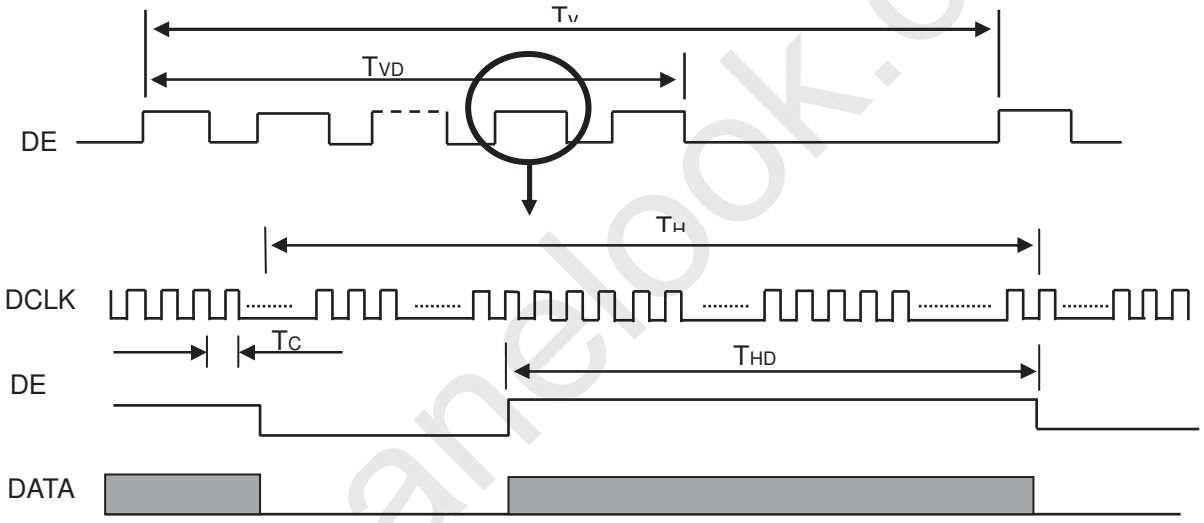
7.1 INPUT SIGNAL TIMING SPECIFICATIONS

The specifications of input signal timing are as the following table and timing diagram.

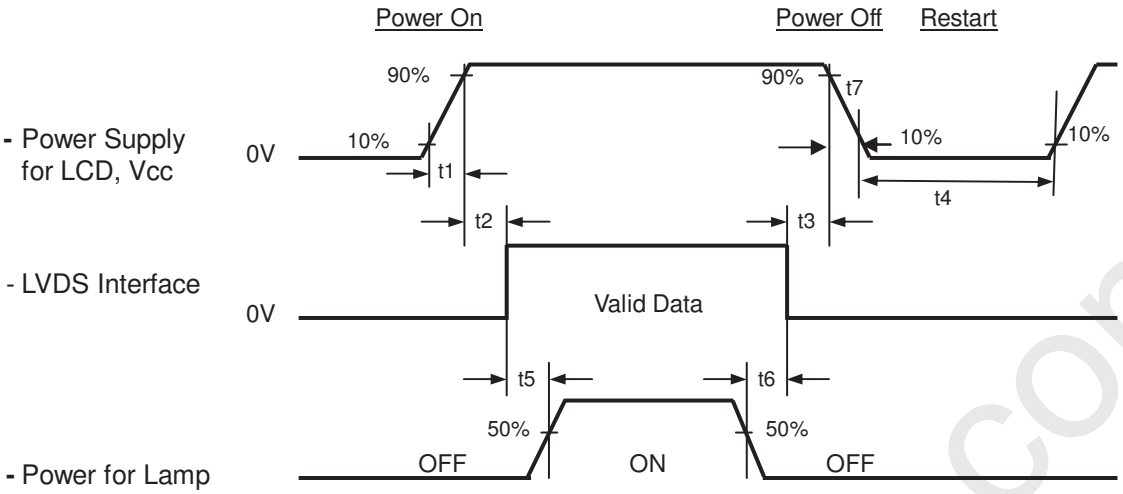
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	50	71	80	MHz	-
DE	Vertical Total Time	TV	803	823	1028	TH	-
	Vertical Addressing Time	TVD	800	800	800	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	23	TV-TVD	TH	
	Horizontal Total Time	TH	1362	1440	1800	Tc	-
	Horizontal Addressing Time	THD	1280	1280	1280	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	

Note (1) Because this open cell is operated by DE only mode, Hsync and Vsync are ignored.

INPUT SIGNAL TIMING DIAGRAM



7.2 POWER ON/OFF SEQUENCE



Timing Specifications:

0.5 ≦ t1 ≦ 10 ms

0 ≦ t2 ≦ 50 ms

0 ≦ t3 ≦ 50 ms

t4 ≧ 500 ms

t5 ≧ 200 ms

t6 ≧ 200 ms

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD open cell might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight converter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight converter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 5≦t7≦300 ms.

8 OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.4	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		

8.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

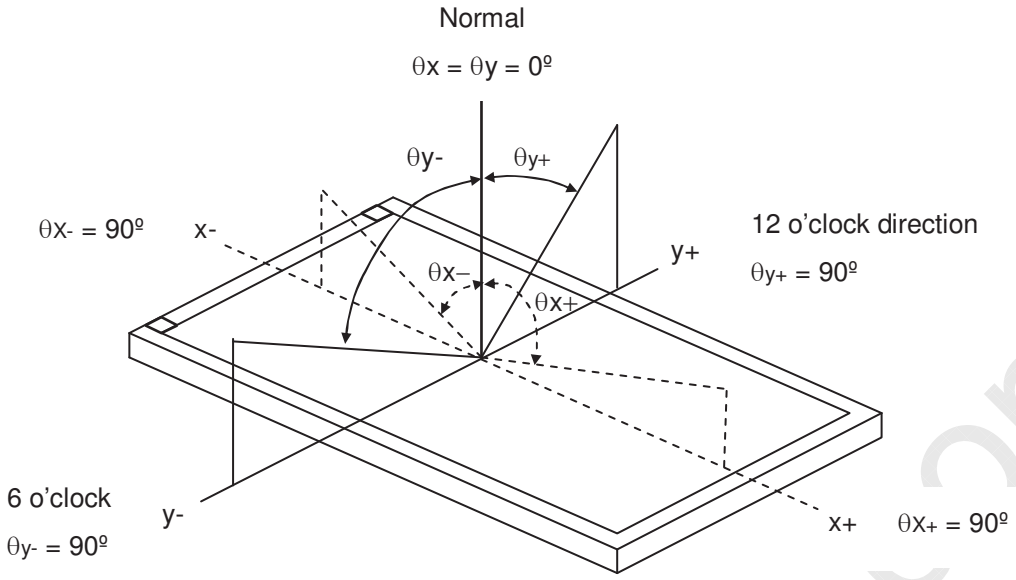
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° CS-1000T Standard light source "C"	Typ - 0.05	0.601	Typ + 0.05	-	(0),(6)
		Rcy			0.329		-	
	Green	Gcx			0.286		-	
		Gcy			0.547		-	
	Blue	Bcx			0.141		-	
		Bcy			0.176		-	
	White	Wcx			0.303		-	
		Wcy			0.350		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0° CS-1000T, CMO BLU	5.6	7	-		(1), (8)
Contrast Ratio		CR		200	300	-	-	(1), (3)
Response Time		T_R	θ_x=0°, θ_Y =0°	-	5	10	ms	(4)
		T_F		-	11	16	ms	
Transmittance uniformity		δT%	θ_x=0°, θ_Y =0° BM-5A	80	90	-	-	(1), (7)
Viewing Angle	Horizontal	θ_x+	CR≥10 BM-5A	40	45	-	Deg.	(1), (3) (6)
		θ_x-		40	45	-		
	Vertical	θ_Y+		15	20	-		
		θ_Y-		40	45	-		

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following：

1. Measure Module's and BLU's spectrums. White is without signal input and R, G, B are with signal input. BLU is supplied by CMO.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (1) Light source is the BLU which is supplied by CMO and driving voltages are based on suitable gamma voltages. White is without signal input and R, G, B are with signal input. SPEC is judged by CMO's golden sample.

Note (2) Definition of Viewing Angle (θx, θy):



Note (3) Definition of Contrast Ratio (CR):

CR_{AVE}= [CR(1)+ CR(2)+ CR(3)+ CR(4)+ CR(5)] / 5

CR_{max}=Max value of CR at whole Viewing Angle

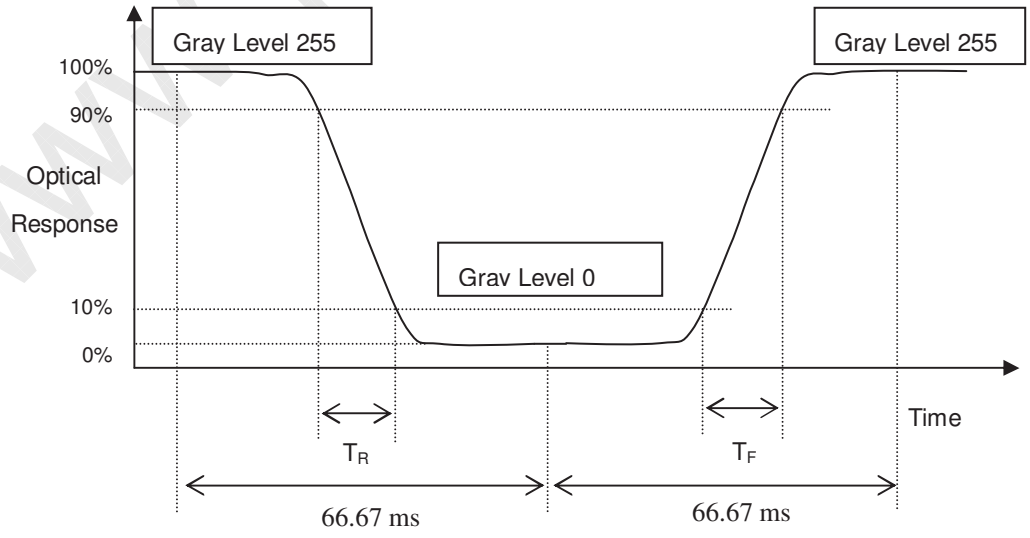
CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

$$CR = \frac{\text{Luminance with all pixel white (Gmax)}}{\text{Luminance with all pixel black (Gmin)}}$$

Gmax: Luminance of gray max at the center point of panel.

Gmin: Luminance of gray min at the center point of panel.

Note (4) Definition of Response Time (T_R, T_F):



Note (5) Definition of Luminance of White (L_C):

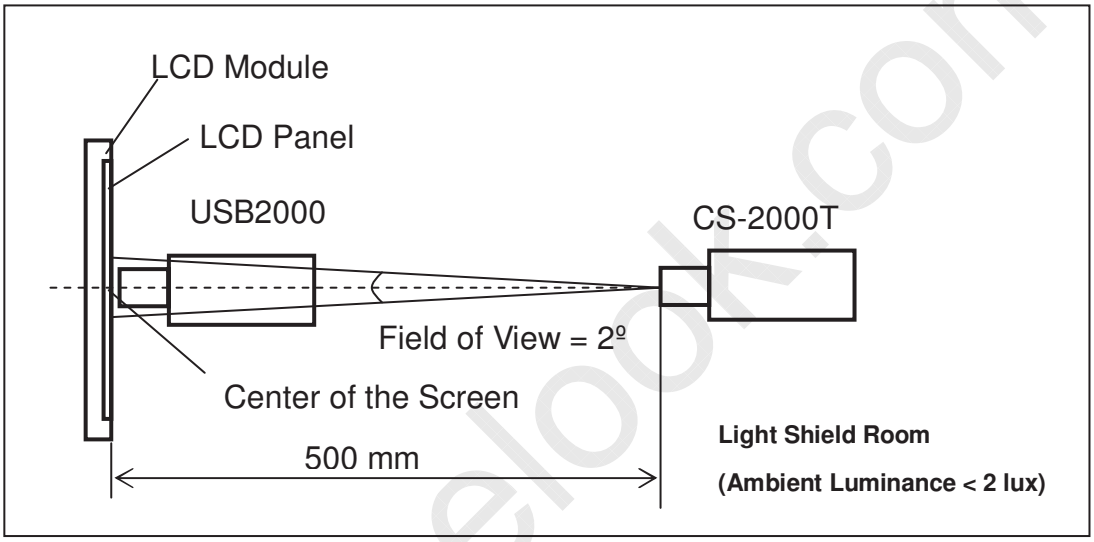
Measure the luminance of gray level 255 at center point

$L_C = L(5)$

L (x) is corresponding to the luminance of the point X at Figure in Note (7).

Note (6) Measurement Setup:

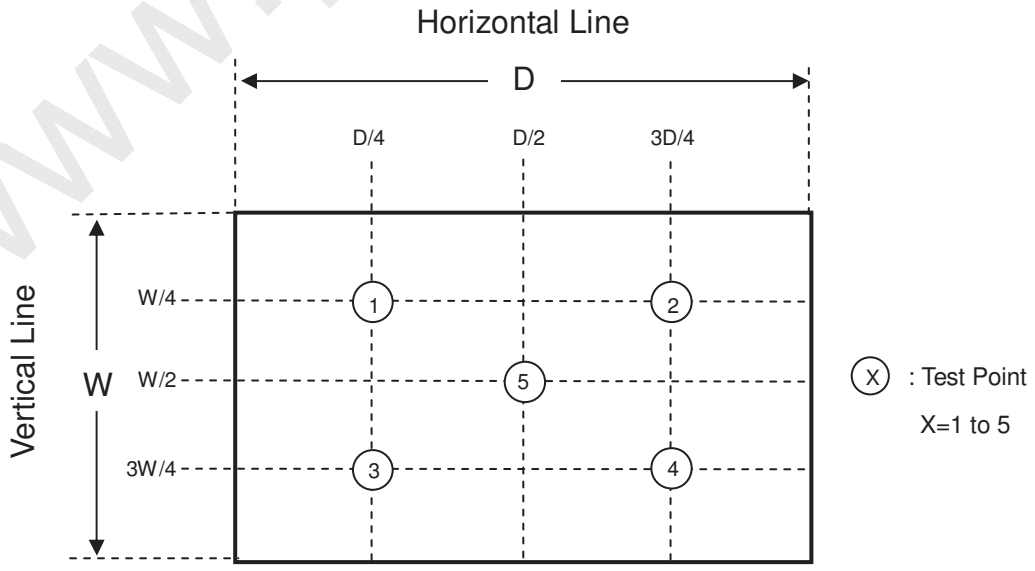
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (7) Definition of Transmittance Variation (δT%):

Measure the transmittance at 5 points

$$\delta T\% = \frac{\text{Minimum } [T\%(1), T\%(2), \ldots T\%(5)]}{\text{Maximum } [T\%(1), T\%(2), \ldots T\%(5)]}$$



Note (8) Definition of Transmittance (T%):

Module is without signal input.

BLU is supplied by CMO.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

9. PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the open cell during assembly.

(2) To assemble or install open cell into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the open cell because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD open cell is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the open cell is operating.

(6) Do not disassemble the open cell.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD open cell, because moisture may damage LCD open cell when it is operating.

(9) High temperature or humidity may reduce the performance of open cell. Please store LCD open cell within the specified storage conditions.

(10) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

9.2 SAFETY PRECAUTIONS

(1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the open cell or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the open cell's end of life, it is not harmful in case of normal operation and storage.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the open cell is operating.

(2) Always follow the correct power on/off sequence when LCD open cell is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

10. PACKAGING

10.1 PACKING SPECIFICATIONS

(1) 56 open cells / 1 Box

(2) Box dimensions: 650mm(L) X 495mm(W) X 320mm(H)

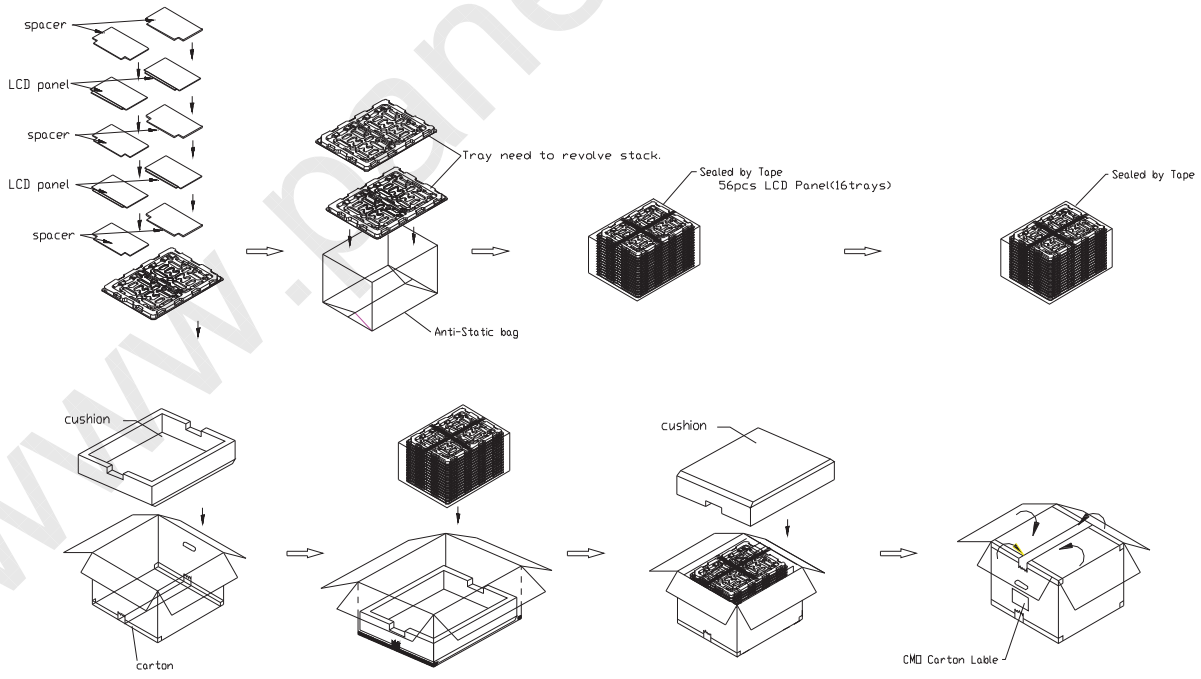
(3) Weight: approximately 12.3Kg (56 open cells per box)

10.2 PACKING METHOD

(1) Carton Packing should have no failure in the following reliability test items

Test Item	Test Conditions	Note
Packing Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (+Z), 10 min (-Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation

(2) Packing method.



(1) Carton Dimensions: 650(L)x495(W)x320(H)mm

(2) 56 LCD Cells+PCB/Carton

10.2 Pallet:

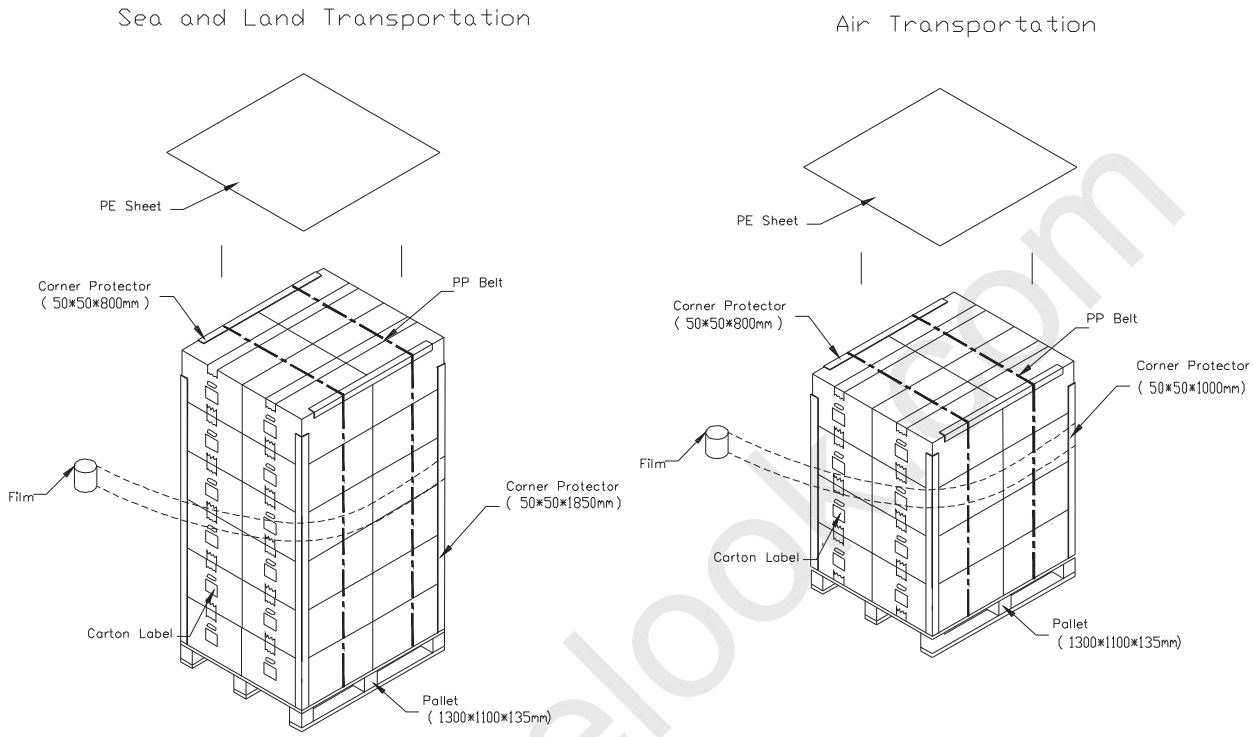


Figure. 10-2 Packing method

11. DEFINITION OF LABELS

11.1 CMO OPEN CELL LABEL

The barcode nameplate is pasted on each OPEN CELL as illustration for CMO internal control.

Barcode definition:

Serial ID: CM-13I62-X-X-X-XX-L-XX-L-YMD-NNNN

Code	Meaning	Description
CM	Supplier code	CMO=CM
13I6A	Model number	N133I6-P0A=13I6A
X	Revision code	C1:1 ,C2:2……
X	Source driver IC code	Century=1, CLL=2, Demos=3, Epson=4, Fujitsu=5, Himax=6, Hitachi=7, Hynix=8, LDI=9, Matsushita=A, NEC=B, Novatec=C, OKI=D, Philips=E, Renasas=F, Samsung=G, Sanyo=H, Sharp=I, TI=J, Topro=K, Toshiba=L, Windbond=M
X	Gate driver IC code	
XX	Cell location	Tainan, Taiwan=TN
L	Cell line #	0~12=1~C
XX	Module location	Tainan, Taiwan=TN
L	Module line #	0~12=1~C
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4… Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31= 1, 2, 3, ~, 9, A, B, C, ~, T, U, V
NNNN	Serial number	Manufacturing sequence of product

11.2 CMO CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation

(a) Model Name: N133I6 –P0A

(b) Carton ID: CMO internal control

(c) Quantities: 56